

What is claimed is:

1. A semiconductor device comprising:

a semiconductor chip which has a main surface, a rear surface, and a plurality of electrodes formed on the main surface;

a plurality of inner leads arranged around the semiconductor chip;

a plurality of outer leads formed integral with the plurality of inner leads, respectively;

a plurality of bonding wires which connect the plurality of electrodes and the plurality of inner leads, respectively; and

a resin encapsulated material which encapsulates the semiconductor chip, the plurality of inner leads, and the plurality of bonding wires,

wherein the portion in which the plurality of inner leads and the plurality of bonding wires are connected are arranged in a zigzag pattern, and

the portion in which the plurality of inner leads and the plurality of bonding wires are connected is fixed to the substrate encapsulated inside the resin encapsulated material via an adhesive layer.

2. A semiconductor device comprising:

a semiconductor chip which has a main surface, a rear surface, and a plurality of electrodes formed on the main surface;

a plurality of inner leads arranged around the

semiconductor chip;

a plurality of outer leads formed integral with the plurality of inner leads, respectively;

5 a plurality of bonding wires which connect the plurality of electrodes and the plurality of inner leads, respectively; and

a resin encapsulated material which encapsulates the semiconductor chip, the plurality of inner leads, and the plurality of bonding wires,

10 wherein the portion in which the plurality of inner leads and the plurality of electrodes are connected are arranged in a zigzag pattern, and

the portion in which the plurality of inner leads and the plurality of bonding wires are connected is fixed to the substrate encapsulated inside the resin encapsulated material via an adhesive layer.

3. A semiconductor device comprising:

20 a first circuit section formed to be including a transistor which has a current passage between the first potential and the second potential;

a second circuit section formed to be including a transistor which has a current passage between the third potential and the fourth potential;

25 a first pad that supplies the first potential to the first circuit section;

a second pad that supplies the second potential to the first circuit section;

a third pad that supplies the third potential to the second circuit section;

a fourth pad that supplies the fourth potential to the second circuit section;

5 a chip that contains the first and the second circuit portions; and

a first lead which is arranged between a plurality of inner leads and supplies the first potential to the first circuit section.

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4. The semiconductor device according to claim 3 wherein the first lead and the first pad are connected by a wire.

5. The semiconductor device according to claim 4 further
15 comprising a chip that contains the first and the second circuit sections and a second lead which is arranged between the plurality of inner leads and supplies the third potential to the second circuit section.

20 6. The semiconductor device according to claim 3 comprising a plurality of the first and the second pads.

7. The semiconductor device according to claim 3 wherein the first lead is connected to the inner lead by a wire, to
25 which the first potential is supplied.

8. The semiconductor device according to claim 3 wherein the first lead has the first inner lead section to which the

first potential is supplied.

9. The semiconductor device according to claim 3 wherein the first circuit section is a digital circuit and the second
5 circuit section is an analog circuit.

10. The semiconductor device according to claim 3 wherein the semiconductor chip containing the first and the second circuit sections and the first to fourth pads, the plurality
10 of inner leads, and the first lead are encapsulated by resin.

11. A semiconductor device comprising:

a first circuit section formed to be including a transistor which has a current passage between the first
15 potential and the second potential included;

a second circuit section formed to be including a transistor which has a current passage between the third potential and the fourth potential;

a first pad that supplies the first potential to the
20 first circuit section;

a second pad that supplies the second potential to the first circuit section;

a third pad that supplies the third potential to the second circuit section;

25 a fourth pad that supplies the fourth potential to the second circuit section;

a first bus-bar arranged along the direction where the first pad and the second pad are arranged, arranged between a

plurality of inner leads and the first and second pads,
connected to the first pad by a wire, and supplied with the
first potential;

5 a second bus-bar arranged along the direction where the
first pad and the second pad are arranged, arranged between a
plurality of inner leads and the first and second pads,
connected to the second pad by a wire, and supplied with the
second potential;

10 a third bus-bar arranged along the direction where the
third pad and the fourth pad are arranged, arranged between a
plurality of inner leads and the third and fourth pads,
connected to the third pad by a wire, and supplied with the
third potential; and

15 a fourth bus-bar arranged along the direction where the
third pad and the fourth pad are arranged, arranged between a
plurality of inner leads and the third and fourth pads,
connected to the fourth pad by a wire, and supplied with the
fourth potential.

20 12. The semiconductor device according to claim 11, wherein
the first bus-bar has the first inner lead section supplied
with the first potential and the third bus-bar has the third
inner lead section supplied with the third potential.

25 13. The semiconductor device according to claim 12, wherein
the second bus-bar has the second inner lead section supplied
with the second potential and the fourth bus-bar has fourth
inner lead section supplied with the fourth potential.

14. The semiconductor device according to claim 12, wherein the second bus-bar is connected to the inner lead by a wire, to which the second potential is supplied, and the fourth bus-
5 bar is connected to the inner lead by a wire, to which the fourth potential is supplied.

15. The semiconductor device according to claim 11 further comprising:

10 a fifth pad for supplying a fifth potential to the first circuit section; and

a fifth bus-bar arranged along the direction where the first pad, the second pad, and the fifth pad are arranged, arranged between a plurality of inner leads and the fifth pad,
15 connected to the fifth pad by a wire, and supplied with the fifth potential.

16. The semiconductor device according to claim 15 further comprising:

20 a sixth pad for supplying a sixth potential to the second circuit section; and

a sixth bus-bar arranged along the direction where the third pad, the fourth pad, and the sixth pad are arranged, arranged between a plurality of inner leads and the sixth pad,
25 connected to the sixth pad by a wire, and supplied with the sixth potential.

17. The semiconductor device according to claim 16, wherein

the fifth bus-bar is connected to the inner lead by a wire, to which the fifth potential is supplied, and the sixth bus-bar is connected to the inner lead by a wire, to which the sixth potential is supplied.

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18. The semiconductor device according to claim 11, wherein the first circuit section is a digital circuit and the second circuit section is an analog circuit.

10 19. The semiconductor device according to claim 11, comprising a plurality of the first and the fourth pads.

20. The semiconductor device according to claim 11 wherein the semiconductor chip that contain the first and the second
15 circuit sections and the first to fourth pads, the plurality of inner leads, the first to the fourth bus-bars, and the wire are encapsulated by resin.

21. The semiconductor device according to claim 11 wherein
20 the second circuit section is arranged much more away from the first and the second bus-bars than the first circuit section and the third pad is contained in the second circuit section.

22. The semiconductor device according to claim 11 wherein
25 the second circuit section is connected to the third pad by a wire, contains the fifth pad that supplies the third potential to the second circuit section, and is arranged much more away from the first and the second bus-bars than the first circuit

section.

23. A semiconductor device comprising:

a first circuit section formed to be including a
5 transistor which has a current passage between the first
potential and the second potential;

a second circuit section formed to be including a
transistor which has a current passage between the third
potential and the fourth potential;

10 a plurality of inner leads;

a first pad that supplies the first potential to the
first circuit section;

a second pad that supplies the second potential to the
first circuit section;

15 a third pad that is connected to the inner lead
supplied with the third potential of the plurality of inner
leads by a wire and supplies the third potential to the second
circuit section;

a fourth pad that that is connected to the inner lead
20 supplied with the fourth potential of the plurality of inner
leads by a wire and supplies the fourth potential to the
second circuit section;

a first ring-form bus-bar going around the outside of a
chip containing the first and the second circuit sections and
25 the first and the fourth pads and connected to the first pad
and an inner lead supplied with the first potential of the
plurality of inner leads by a wire; and

a second ring-form bus-bar going around the outside of

the first ring-form bus-bar, connected to the second pad by a wire, and having an inner lead section to which the second potential is supplied.

5 24. The semiconductor device according to claim 23, further comprising:

 a fifth pad that supplies the fifth potential to the first circuit section; and

 a third ring-form bus-bar going around the outside of a
10 chip containing the first and the second circuit sections and the first and the fourth pads and connected to the fifth pad and an inner lead supplied with the fifth potential of the plurality of inner leads by a wire.

15 25. The semiconductor device according to claim 23, wherein the first circuit section is a digital circuit and the second circuit section is an analog circuit.

 26. The semiconductor device according to claim 23,
20 comprising a plurality of the first and the fourth pads.

27. A semiconductor device, comprising:

 a first and a second pads arranged on a first row along the side of a semiconductor chip;

25 a first inner lead of a plurality of inner leads arranged to surround the semiconductor chip, which is connected to the first pad by a first wire;

 a second inner lead of the plurality of inner leads,

which is adjacent to the first inner lead and is connected to the second pad by a second wire;

a third pad located on a second row along the side of the semiconductor chip and between the first pad and the

5 second pad; and

a first bus-bar arranged along the semiconductor chip and between the semiconductor chip and the first and second inner leads;

10 wherein the third pad is connected to the first bus-bar by a third wire that passes between the first wire and the second wire.

28. The semiconductor device according to claim 27, wherein the first and the second pads are primarily pads for signals,
15 the third pad is primarily a pad for supplying the power potential, and the first row is arranged nearer on the edge side of the semiconductor chip than the second row.

29. The semiconductor device according to claim 27, wherein
20 the first and the second pads are primarily pads for signals, the third pad is primarily a pad for supplying the power potential, and the first row is arranged inner on the edge side of the semiconductor chip than the second row.

25 30. The semiconductor device according to claim 27, wherein the first and the second pads are repeatedly arranged on the first row and the third pad is repeatedly arranged on the second row, thereby forming zigzag-pattern pad arrangement.

31. A semiconductor device, comprising:

a plurality of inner leads arranged to surround a semiconductor chip;

5 a plurality of input/output pads arranged on the first row of the semiconductor chip and connected to the plurality of inner leads by wires;

a first bus-bar arranged along the direction of the first row and between the semiconductor chip and the plurality
10 of inner leads, and supplied with the first potential;

a second bus-bar arranged along the direction of the first row and between the semiconductor chip and the plurality of inner leads and supplied with the second potential; and

a plurality of the first and the second power supply
15 pads arranged between each of the plurality of input/output pads and connected to the first and the second bus-bars by wires;

wherein the input/output pads, the first power supply pad, the input/output pads, the second power supply power are
20 arranged in that order.

32. A semiconductor device, comprising:

a first circuit section containing a transistor which has a current passage between the first potential and the
25 second potential;

a second circuit section containing a transistor which has a current passage between the third potential and the fourth potential and has a step-down circuit;

a first pad that supplies the first potential to the first circuit section;

a second pad that supplies the second potential to the first circuit section;

5 a first selection pad connected to the step-down circuit by wiring;

a second selection pad connected to the step-down circuit by wiring;

10 a plurality of inner leads arranged so as to surround a semiconductor chip containing the first and the second circuits;

a first bus-bar arranged between the semiconductor chip and a plurality of inner leads, connected to the first pad by a wire, and supplied with the first potential;

15 a second bus-bar arranged between the semiconductor chip and a plurality of inner leads, connected to the second pad by a wire, and supplied with the second potential; and

a third bus-bar arranged between the semiconductor chip and a plurality of inner leads, connected to the third pad by
20 a wire, and supplied with the third potential;

wherein, when the first selection pad is connected to the first bus-bar by wire-bonding, the step-down circuit steps down the first potential and supplies the third potential to the second circuit, and

25 when the second selection pad is connected to the third bus-bar by wire-bonding, the third potential is supplied from the third bus-bar to the second circuit section without through passing the step-down circuit.

33. A semiconductor device, comprising:

a first circuit section formed to be including a transistor which has a current passage between the first potential and the second potential;

a second circuit section formed to be including a transistor which has a current passage between the third potential and the fourth potential;

a plurality of inner leads;

a first pad that supplies the first potential to the first circuit section;

a second pad that supplies the second potential to the first circuit section;

a third pad that supplies the third potential to the second circuit section;

a fourth pad that supplies the fourth potential to the second circuit section;

a first ring-form bus-bar arranged so as to surround the outer circumference of a chip containing the first and the second circuit sections and the first and the fourth pads and connected to the first and the third pads by wires; and

a second ring-form bus-bar arranged so as to surround the outer circumference of a chip containing the first and the second circuit sections and the first and the fourth pads and connected to the second and the fourth pads by wires;

wherein the first ring-form bus-bar is electrically isolated by providing a notch between the portion where the first pad comes in contact with and the portion where the

third pad comes in contact with, and

the second ring-form bus-bar is electrically isolated by providing a notch between the portion where the second pad comes in contact with and the portion where the fourth pad comes in contact with.

34. The semiconductor device according to claim 33, wherein the portion where the first pad of the first ring-form bus-bar comes in contact with has an inner lead section to which the first potential is supplied;

the portion where the third pad of the first ring-form bus-bar comes in contact with has an inner lead section to which the third potential is supplied;

the portion where the second pad of the first ring-form bus-bar comes in contact with is connected by the inner lead to which the second potential is supplied and a wire; and

the portion where the fourth pad of the second ring-form bus-bar comes in contact with is connected by the inner lead to which the forth potential is supplied and a wire.

35. The semiconductor device according to claim 34, further comprising:

a fifth pad for supplying the fifth potential to the first circuit;

a sixth pad for supplying the sixth potential to the second circuit; and

a third ring-form bus-bar arranged so as to surround the outer circumference of a chip containing the first and the

second circuit sections as well as the first and the fourth pads and connected to the fifth and the six pads by wires;

wherein the third ring-form bus-bar is electrically isolated by providing a notch between the portion to which the fifth pad is connected and the portion where the sixth pad is connected.

36. The semiconductor device according to claim 35, wherein the portion to which the fifth pad of the third ring-form bus-bar is connected is connected by an inner lead to which the fifth potential is supplied and a wire, and the portion to which the sixth pad of the third ring-form bus-bar is connected is connected by an inner lead to which the sixth potential is supplied and a wire.

37. The semiconductor device according to claim 33, wherein the first circuit section is a digital circuit and the second circuit section is an analog circuit.

38. The semiconductor device according to claim 33, comprising a plurality of the first and the fourth pads.

39. The semiconductor device according to claim 33, wherein the semiconductor chips that contain the first and the second circuit sections and the first to fourth pads, the plurality of inner leads, the first and the second ring-form bus-bars, and the wire are encapsulated by resin.

40. A semiconductor device, comprising:

a semiconductor chip having a main surface and a rear surface;

a plurality of inner leads and outer leads; and

5 a pair of bus-bars arranged along the semiconductor chip;

wherein the semiconductor chip comprises electrodes formed on the main surface for a first and a second power supply potentials; and

10 a circuit electrically connected to one bus-bar via the electrode for the first power supply potential, and further electrically connected to the other bus-bar via the electrode for the second power supply potential; and

15 to each of the pair of bus-bars, the outer lead is coupled, respectively, and the outer leads respectively coupled to the pair of bus-bars are arranged adjacently.

41. The semiconductor device according to claim 40, wherein the circuit is either analog circuit or a differential
20 amplifier circuit.

42. The semiconductor device according to claim 41, wherein the analog circuit receives a supply of reference-level potential from the outside.

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43. A semiconductor device, comprising:

a semiconductor chip having a main surface and a rear surface;

a plurality of inner leads and outer leads; and
a pair of bus-bars arranged along the semiconductor
chip;

wherein the semiconductor chip comprises electrodes
5 formed on the main surface for a first and a second power
supply potentials and an electrode for signals; and

a circuit electrically connected to one bus-bar via the
electrode for the first power supply potential, and further
electrically connected to the other bus-bar via the electrode
10 for the second power supply potential; and

to each of the pair of bus-bars, the outer lead is
coupled, respectively, and the outer leads coupled
respectively to the pair of bus-bars are arranged on the
opposite side with an outer lead electrically connected to the
15 electrode for signals being positioned therebetween.

44. A semiconductor device, comprising:

a semiconductor chip having a main surface, a rear
surface, and a plurality of electrodes formed on the main
20 surface;

a plurality of inner leads arranged on the
circumference of the semiconductor chip;

a plurality of outer leads formed integral with the
plurality of inner leads, respectively;

25 a plurality of bonding wires that connect the plurality
of electrodes and the plurality of inner leads, respectively;

a sheet-form chip mounting section connected to the
semiconductor chip; and

tape members that connect each of the head ends of the plurality of inner leads to the chip mounting section;

wherein the chip mounting section is smaller than the main surface of the semiconductor chip.

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45. A semiconductor device, comprising:

a semiconductor chip having a main surface, a rear surface, and a plurality of electrodes formed on the main surface;

10 a plurality of inner leads arranged on the circumference of the semiconductor chip;

a plurality of outer leads formed integral with the plurality of inner leads, respectively;

15 a plurality of bonding wires that connect the plurality of electrodes and the plurality of inner leads, respectively;

a sheet-form chip mounting section connected to the semiconductor chip; and

tape members that connect each of the head ends of the plurality of inner leads to the chip mounting section;

20 wherein the chip mounting section is larger than the main surface of the semiconductor chip.

46. A semiconductor device, comprising:

25 a semiconductor chip having a main surface and a rear surface;

a plurality of inner leads and outer leads;

a pair of bus-bars arranged along the semiconductor chip; and

a resin encapsulated material for encapsulating the semiconductor chip and the plurality of inner leads;

wherein the outer lead is coupled to the pair of bus-bars, respectively.

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47. The semiconductor device according to claim 46, wherein the outer leads coupled to the pair of bus-bars, respectively, are arranged adjacently.

10 48. The semiconductor device according to claim 46, wherein the outer leads coupled to the pair of bus-bars, respectively, are arranged at corners of the resin encapsulated material.

49. The semiconductor device according to claim 46, wherein
15 the outer leads coupled to the pair of bus-bars, respectively, are arranged at the center in the lead aligned direction on the side surface of the resin encapsulated material.

50. The semiconductor device according to claim 46, wherein
20 the outer leads coupled to the pair of bus-bars, respectively, are arranged at four corners of the resin encapsulated material.

51. The semiconductor device according to claim 46, wherein
25 the outer leads coupled to the pair of bus-bars, respectively, are protruded from a plurality of places on the side surface of the resin encapsulated material.